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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,626	11/30/2004	Bernardo De Oliveira Kastrup Pereira	NL02 0444 US	6975

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EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2181	

MAIL DATE	DELIVERY MODE
09/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/516,626	DE OLIVEIRA KASTRUP PEREIRA, BERNARDO	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: request for continued examination received on 06/19/2007.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/19/2007 has been entered.

4. Regarding the amendments to the claims, the examiner notes that 37 CFR 1.121 requires that "the text of any deleted matter must be shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters". Amendments to the claims show text that is not five or fewer consecutive characters enclosed by double brackets. For the purposes of examination, the text enclosed by double brackets will be interpreted as deleted as this appears to what the applicant intended.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by DeHon et al., U.S. Patent No. 5,956,518 (Hereinafter DeHon).

7. Referring to claims 1 and 9, taking claim 1 as exemplary, DeHon has taught an integrated circuit comprising:

a plurality of processing elements *[basic functional units (BFUs); component 100]* for executing in parallel at least a subset of a plurality of instructions *[Fig. 4; column 5, lines 3-10, 44-48]*;

issuing means *[F BFUs; See Fig. 4]* for configuring the plurality of processing elements by issuing a program-counter-driven instruction flow *[from the PC BFU; See Fig. 4]* to the plurality of processing elements *[column 5, lines 16-23, 44-48]*; and

configurable interconnection *[programmable interconnect; component 101]* means for connecting each processing element from the plurality of processing elements to at least a subset of other processing elements from the plurality of processing elements *[Fig. 4; column 5, lines 3-10]*;

characterized in that:

the processing elements from the plurality of processing elements are similar to each other, each processing element from the plurality of processing elements being capable of executing each instruction from the plurality of instructions as issued by the issuing means *[column 5, lines 3-10]*; and

the plurality of processing elements are laid out in a regular grid wherein a distance between a processing element and a neighboring processing element from the plurality of processing elements in a first direction is the same as a distance between the processing element and a neighboring processing element from the plurality of processing elements in a second direction that is different from the first direction *[See Fig. 8; column 8, lines 17-21, 31-37]*.

8. Referring to claim 2, DeHon has taught an integrated circuit as claimed in claim 1, wherein the integrated circuit comprises a very long instruction word processor architecture and the subset of the plurality of instructions comprises a very long instruction word *[column 5, lines 44-48]*.

9. Referring to claims 3 and 10, taking claim 3 as exemplary, DeHon has taught an integrated circuit as claimed in claim 1, characterized in that the configurable interconnection means connect each processing element to each nearest neighboring processing element in the grid *[column 8, lines 23-30]*.

10. Referring to claim 4, DeHon has taught an integrated circuit as claimed in claim 1, characterized in that the configurable interconnection means comprise bypassing means for bypassing a processing element from the plurality of processing elements *[column 8, lines 38-51]*.

11. Referring to claim 5, DeHon has taught an integrated circuit as claimed in claim 1, characterized in that a processing element *[BFU]* from the plurality of processing elements comprises a data storage unit *[memory block; Fig. 6, component 110]*, a function unit *[ALU core; Fig. 6, component 120]* and an internal intercommunication

network *[Fig. 6]* coupling the function unit to the data storage unit *[column 5, line 57 – column 6, line 4]*.

12. Referring to claim 6, DeHon has taught an integrated circuit as claimed in claim 5, characterized in that the processing element comprises at least a further unit *[MUX; Fig. 6, component 126]*; the function unit, the further unit and the data storage unit being organized as a very long instruction word processor data path *[When the device is configured to be a very long instruction word (VLIW) system, the MUX, the ALU, and the memory block are all part of the a VLIW processor data path (column 5, lines 44-48; Fig. 4)]*.

13. Referring to claim 7, DeHon has taught an integrated circuit as claimed in claim 6, characterized in that the issuing means are distributed over the processing elements *[There are multiple F BFUs. Therefore, the issuing means are distributed over the processing elements (BFUs); See Fig. 4; column 5, lines 44-48]*.

14. Referring to claim 8, DeHon has taught a data processing device having an input for receiving a digital data stream and having an output for transmitting a humanly perceptible data result resulting from the digital data stream, characterized in that the input is coupled to the output via an integrated circuit as claimed in claim 1, the integrated circuit being arranged for extracting the data result from the digital data stream *[Fig. 22; column 13, lines 49-67]*.

Response to Arguments

15. Applicant's arguments filed 06/19/2007 have been fully considered but they are not persuasive.

16. Applicant argues the novelty/rejection of claims 1-10 on pages 5-7 of the remarks, in substance that:

> "DeHon clearly fails to teach or suggest an issuing means for configuring basic functional units BFU 100 by issuing a program-counter driven instruction flow to basic functional units BFU 100 as encompassed by independent claims 1 and 9. As such, DeHon clearly fails to teach or suggest a design and incorporation of each basic functional unit BFU 100 to be capable of executing each instruction from the plurality of instructions by the issuing means as required by independent claims 1 and 9." (page 6)

These arguments are not found persuasive for the following reasons:

DeHon states that the F BFUs control operations performed by ALUs (column 5, lines 16-19). That is, DeHon has taught an issuing means (i.e. F BFUs) that issue operations (i.e. instructions) to the ALUs. DeHon further states that these instructions are program counter driven (column 5, lines 21-22) and are capable of being executed by any of the BFUs (column 5, lines 11-16). Therefore, DeHon has taught an "issuing means for configuring the plurality of processing elements by issuing a program-counter-driven instruction flow to the plurality of processing elements" where "each processing element from the plurality of processing elements being capable of executing each instruction from the plurality of instructions as issued by the issuing means" as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib
Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER